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PATENT AND TRADEMARK OFFICE

Patent No.	:	6,882,312	Confirmation No. 2379
Issued	:	April 19, 2005	
Appl. No.	:	10/806,781	
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Docket No.	:	1010-0002-USA	
Title	:	METHOD AND APPARATUS FOR MULTIPATH MITIGATION USING ANTENNA ARRAY	

Attention: Certificate of Corrections Branch
Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450.

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 CFR 1.322

Patentee hereby requests a Certificate of Correction under 37 CFR 1.322 in order to correct PTO mistakes in the above identified patent.

The text of the requested corrections are set forth in the enclosed Certificate of Correction form PTO/SB/44, with the location of the errors in the printed patent identified by column/claim and line numbers.

The requested corrections were incurred through the fault of the PTO. This request is supported by documentation showing that the requested corrections were included in the application as filed. This documentation includes copies of the relevant pages of the application as filed as well as a cross reference identifying the location of each error in the patent and its corresponding location in the application as filed.

I hereby certify that this correspondence, as well as any items referred to as being transmitted herewith, is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on May 6, 2005.

Typed or printed name of person signing this certificate: Risa Garcia

Signature: Risa Garcia

Expedited processing of this Request is hereby requested.

Respectfully,

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Dated: May 6, 2005

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,882,312

DATED : April 19, 2005

INVENTOR(S) : Michael Yu. Vorobiev, Mark I. Zhodzishsky, Andrew V. Veitsel, Victor A. Veitsel, Alexey V. Zhdanov, Sergey N. Pushkarev

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 7, line 65, "p jw", should read --p=jw--.

Column 9, line 45, "AE_2 **106**. AE_m **108**", should read --AE_2 **106** … AE_m **108**--.

Column 12, line 66, the equation in claim 15 should read --$\varphi_{ik} = (2\pi L_i / \lambda) \sin \theta_k$--.

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PATENT NO. 6,882,312

No. of additional copies

MAY 16 2005

CROSS-REFERENCE OF ERRORS IN PATENT WITH LOCATION IN APPLICATION AS FILED

REQUEST FOR CORRECTION	LOCATION OF CORRECT TEXT IN APPLICATION AS FILED
Column 7, line 65, "p jw", should read --p=jw--..	Paragraph 40, lines 6-7
Column 9, line 45, "AE$_2$ **106**. AE$_m$ **108**", should read --AE$_2$ **106** … AE$_m$ **108**--.	Paragraph 49, line 7
Column 12, line 66 the equation in claim 15 should read --$\varphi_{ik} = (2 \pi L_i / \lambda) \sin \theta_k$--.	Page 21, claim 15, line 5

[0040] The PLL unit 410 operates as follows. Samples I and Q from the output of the correlator 402 are provided to the PLL discriminator 412. The PLL discriminator 412 may operate to generate Z=atan (Q/I). The output of the PLL discriminator 412 is provided to the PLL loop filter 414. The PLL loop filter 414 may have the following transfer function: $K(p) = K1 + K2/p + K3/(p*p)$ where K1, K2 and K3 are the coefficients of the proportional, integrating and double integrating filter loops respectively, and $p = jw$, $j = sqrt(-1)$, $w=2\pi f$, and f is the frequency. The coefficients are selected so that the bandwidth of the filter would be 10...50 Hz.

[0041] The controlling signal output by the PLL loop filter 414 in addition to being provided to the navigation processor 132 for the navigation task, is further provided to a carrier numerical controlled oscillator (NCO) 406, which generates the appropriate frequency of the carrier reference signal for the satellite channel being processed by the satellite channel processor 400. This frequency will be different for each of the satellite channel processors shown in Fig. 1 because each satellite channel processor tracks one specific satellite in view of the antenna array 102. The signals from the output of the PLL loop filter 414 contain the information about the difference in the carrier phase of the received and reference signals. This difference is continuously applied to the NCO 406 in order to correct the NCO and provide phase and frequency coincidence between the reference signal oscillations and carrier signal oscillations.

[0042] The code oscillator 407 generates the appropriate pseudo-random code. The pseudo-random code is selected according to the GPS satellite number (in case of GLONASS the channel frequency number of the reference signal is used) being processed by the particular satellite channel processor 400 in a manner well known to one of ordinary skill in the art.

[0043] The phase shifter 404 adds the phase of NCO 406 to a phase shift correction signal received from the control and synchronization unit 124 as will be described in further detail below. The output of the phase shifter 404 is then provided to the modulator 405 which modulates the sinusoidal signal output from the phase shifter 404 with the pseudo-random code output from the code oscillator 407 to generate the reference signal.

magnetic compass, for example the HMR3000 available from Honeywell, may be used to implement these sensors. The input parameters related to the angles of the antenna elements and the element-to-element distance are known in advance based on the design of the antenna array and may be stored in the attitude unit 138 in advance.

[0047] In an embodiment in which the antenna array 102 is implemented as a linear vertical antenna array with the antenna center on the vertical rod, the phase shift correction module 134 generates a correction phase shift signal (ϕ_{ik}) for the *i-th* antenna element and the *k-th* satellite in accordance with the following equation:

$$\phi_{ik} = (2\,\pi L_i / \lambda) \sin \theta_k$$

where L_i, λ, and θ_k are as described above.

[0048] Further, in a linear vertical antenna array embodiment (e.g., as shown in Fig. 2), it is desirable to block the signals from the bottom antenna element 206 with respect to signals received from satellites having high elevation angles because at high elevation angles the upper antenna 204 shades the bottom antenna, thereby resulting in a deterioration of the signal received at the bottom antenna 206. In this embodiment, the blocking module 136 of the control and synchronization unit 124 generates a blocking signal at the moment when the antenna switch 116 connects the bottom element of the vertical antenna array to the signal processing path, and this blocking signal is provided to the PLL unit 410 and DLL unit 408 of each of the satellite channel processors, thereby disabling the signal from the bottom antenna in the PLL unit 410 and DLL unit 408. The particular satellite elevation angle, above which the bottom antenna element will be blocked, is dependent upon the particular design of the vertical antenna array. In an advantageous embodiment, a suitable threshold angle is 30 ... 45 degrees.

[0049] The operation frequency of the control and synchronization unit 124 is synchronized with the PLL bandwidth. For example, in an embodiment in which the antenna array is implemented as a horizontal planar antenna array with four antenna elements (e.g., as shown in Fig. 3), if the PLL bandwidth is between 20.. 25 Hz, then the

operation period of the control and synchronization unit is equal to 0.8 ms. As described above, the control and synchronization unit 124 controls switch 116 to cyclically connects antenna elements AE_1 104, AE_2 106 ... AE_m 108 to RF cable 122 and the single signal processing path. Simultaneously, the phase shift correction module 134 of the control and synchronization unit 124 generates the phase shift correction signal which is output to the phase shifter 404. The phase shift correction signal is synchronously generated for the particular antenna element of the antenna array that is currently connected to the signaling path. Thus, for example, at the moment when the signal from antenna element AE_1 104 is connected to the single signal processing path, and is being processed by the satellite channel processors, the phase shift correction signal generated for AE_1 104 is provided to the phase shifter 404 of each of the satellite channel processors 400.

[0050] Having described various embodiments of the invention above, a higher level more theoretical discussion of processing in accordance with the embodiments will now be given. The above described embodiments suggests that only satellite signals received by the antenna array elements directly from a satellite, be phased. A correction phase shift is calculated for each antenna array element and each active satellite based on information about the direction to the satellite, the angle attitude of the antenna array, and the configuration of elements in the antenna array. The calculated correction phase shift is added to the PLL reference signal. A common additive signal, which comprises signals of the successively switched antenna elements, arrives at the input of a processing channel for each satellite. The common additive signal contains the direct signal and an interference component including constituents of both noise and reflected (multipath) signals. Both of the interference constituents contribute to the total error budget, although their influence differs. The components of interference signal have different spectra, even though they are both additive and pass through the common signal path.

[0051] Noise is a wide-band process with short correlation time. Hence, noise samples are substantially independent if the phase shift between them is equal to the clock of the antenna switch (where the clock is the time period which is inverse to the

13. The apparatus of claim 12 wherein each of said plurality of satellite channel processors further comprises a phase shifter for receiving said phase shift correction signals and for applying said phase shift correction signals to said reference signal.

14. The apparatus of claim 12 wherein said antennas are implemented as a horizontal antenna array and wherein said phase shift correction signals ϕ_{ik} for an *i-th* antenna and a *k-th* satellite are calculated according to:

$$\phi_{ik} = (2\,\pi L_i / \lambda) \cdot (\cos\theta_k \cos\theta_i \cos(\alpha_k - \alpha_i) + \sin\theta_k \sin\theta_i)$$

where

λ is the wavelength of carrier oscillation;

L_i is the distance between the *i-th* antenna and an antenna center;

θ_i is the elevation angle of a line that connects the antenna center to the *i-th* antenna;

θ_k is the elevation angle of the *k-th* satellite;

α_i is the azimuth of a line that connects the antenna center to the *i-th* element; and

α_k is the azimuth of the *k-th* satellite.

15. The apparatus of claim 12 wherein said antennas are implemented as a vertical antenna array with an antenna center on the vertical axis and wherein said phase shift correction signals ϕ_{ik} for an *i-th* antenna and a *k-th* satellite are calculated according to:

$$\phi_{ik} = (2\,\pi L_i / \lambda) \sin\theta_k$$

where

λ is the wavelength of carrier oscillation;

L_i is the distance between the *i-th* antenna and an antenna center; and

θ_k is the elevation angle of the *k-th* satellite.

16. The apparatus of claim 10 further comprising a blocking module for generating a blocking signal and providing said blocking signal to said plurality of